A Procedure to Back-annotate Process Induced Layout Dimension Changes into the Post Layout Simulation Netlist

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ABSTRACT

As transistor dimensions become smaller, on-wafer transistor dimension variations, induced by lithography or etching process, impact more to the transistor parameters than those from the earlier process technologies such as 90 nm and 130 nm. The on-wafer transistor dimension variations are layout dependent and are ignored in the standard post layout verification flow where the transistor parameters in a spice netlist are extracted from drawn transistor dimensions. There are commercial software tools for predicting the on-wafer transistor dimensions for the improved accuracy of the post-layout verification. These tools need accurate models for the on-wafer transistor dimension prediction and the models need to be re-calibrated as the fabrication process is changed. Furthermore, the model-based predictions of the on-wafer transistor dimensions require extensive computing power which can be time consuming.

In the paper, a procedure to back-annotate the process induced transistor dimension changes into the post layout extracted netlist using a simple look-up table is described. The lookup table is composed of specified drawn transistor and its sounding layout as well as their on-wafer dimensions. The on-wafer dimensions can be extracted from simulations ,SEM in-line pictures or electrical data of specially designed testkeys. Taking the lookup table data, accordingly, the transistor dimensions in the post-layout netlist file are then modified by a commercial software tool with a pattern search function. Comparing with the model based approach, the lookup table approach takes much less time for modifying the post-layout netlist. The lookup table approach is flexible, since the tables can be easily updated to reflect the most recent process changes from the foundry.

In summary, a lookup table based approach for improving the post-layout verification accuracy is described. This approach can improve the verification accuracy from both litho and non-litho process variations. This approach has been applied to Xilinx's 65 nm and 45 nm product developments.

KEYWORDS: DFM, back-annotation, post-layout verification, look-up table, corner rounding, pattern search.

INTRODUCTION

For the early process technologies such as 0.5 um and 0.35 um, layout feature sizes are in the range of 0.35 um to 0.5 um.   The 0.365 um illuminating wavelength of the lithography system is comparable or smaller than the layout feature sizes for these technologies.   Together with large design rules such as gate poly width and bent field poly to diffusion, the design layout printed on wafers can reach desired critical dimension (CD) accuracy, without optical proximity correction (OPC).

Both the illuminating wavelength and layout feature size are shrunk as the process technology evolvement.   However, before the introduction of EUV lithography system with a wavelength reduction from 193 nm (deep UV) to 13.6 nm (EUV), the lithography wavelength stays at 193 nm and is not further reduced [1].   Throughout the process technology development with the 193 nm wavelength lithography systems, the image resolution is enhanced through improved optical system designs such as increased NA and immersion scheme to cop with reduced feature sizes. Together with the help of OPC, these lithography enhancements help to control through-pitch CDs for such technologies as 65 nm and 45 nm well.   With the feature sizes in these technologies, however, line-end shortening and corner rounding are more "distorted" than those for earlier technologies.   OPC can provide some corrections to these patterns, but cannot eliminate the distortions.   For example, with OPC, the poly and diffusion CDs can be corrected to as close to target values as possible and corner rounding and line end loss can only be reasonably compensated for.   Overly corrected line-end loss and corner rounding can cause shorting to the neighboring patterns or line breakage.

These un-corrected residuals (diffusion and poly corner rounding) can result in unexpected changes of transistor dimensions on wafers and therefore their drive currents. These changes are considered as wafer process induced systematic variations. Their impacts to the transistor currents are to be evaluated and to modify (i.e., "annotate") the design information file (i.e., post layout extracted netlist) accordingly.

APPROACH

The diffusion and poly corner rounding contours can be simulated with commercially available lithography simulation software [2, 3].   The contour can be simplified by "tranglularizing" the contour to simplify the transistor current change calculation.   The procedure is illustrated as Figure 2 in which the effective poly width (L_{eff}) is calculated with the following equation

$L_{eff} = b \left(((a+c)/2) + (w-b)a\right)/w$ (Equation 1)

where

w is diffusion width,

a is drawn poly width,

b is poly rounding encroaching diffusion distance, and

c is widened poly width at diffusion edge due to the poly corner rounding.
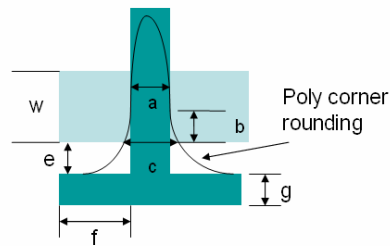

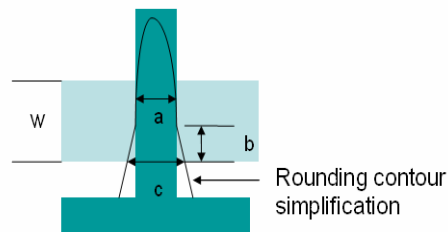Figure 1: Transistor layout parameter definitions and simulated contour illustration.

Figure 2: Simplification of the contour for effective poly width (L_{eff}) calculation.

It can be seen from this equation that

- With a fixed diffusion width, smaller bent field poly-to-diffusion spacing yields larger L_{eff}. This can cause an unexpected reduction of transistor drive current. Also, for certain transistor layouts in the memory, that require transistor matching, under the misalign condition of poly and diffusion layers, this can cause increased transistor mismatch and therefore narrow the circuit operating window. Therefore, a proper design rule needs to be implemented. Also, certain layout styles need to be included as the design for manufacturability (DFM) practice to reduce this problem [4, 5].

- With a fixed bent field-poly-to-diffusion spacing, a larger diffusion width, w, can in effect reduce the poly width variation. This can help to flexibly implement the design rule. For example, for a transistor with poly width of 40 nm and with diffusion width of 100 nm, the bent field poly-to-diffusion spacing needs to be 60 nm to larger. This rule can be tightened as the diffusion width increases, say, from 100 nm to 500 nm.

Evaluation of transistor corner rounding for a large scale of design requires analysis of the layout environment in which OPC performs corner rounding correction differently. For example, OPC generally makes more aggressive corner rounding correction for wide poly than that for narrow poly. Also, OPC makes more corner rounding correction for long bent field poly length than that for short one. Depending

on OPC approach from the wafer foundries, typical OPC corrections for the corner rounding are shown in Figure 3.
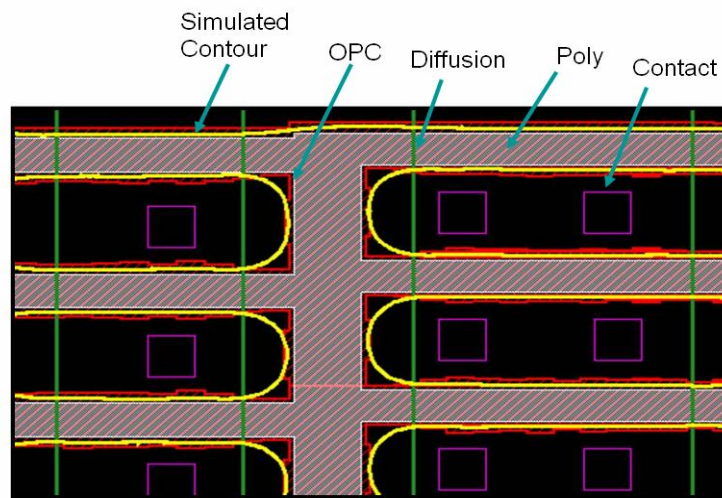

Figure 3: A typical transistor layout with bent field poly, its OPC, and its simulated on-wafer contour.

As another approach, the lookup table can also be generated with transistor structures that are designed in a technology development test vehicle.

THE LOOKUP TABLES

With 65 nm process technology as an example, the sample layout with various transistor structures is sent to wafer foundry for OPC process and then brought it back to the IC design house for corner rounding simulations with its in-house lithography simulation tool.   As illustrated in Figure 1 and with Equation 1, the calculated L_{eff}'s, based on various layout parameters of

- bent field poly width (a),
- bent field poly length (e),
- bent field poly to diffusion spacing (f), and
- bent field poly width (g),

are tabulated in Table 1.

Bent field poly width (g)	Bent field poly length (e)	Transistor poly width (a)	Bent field poly to diffusion spacing (f)	Diffusion width (w)	Effective poly width (Leff)
130	210	70	100	120	76.25
130	210	70	100	150	75.00
130	210	70	100	200	73.75
130	210	70	110	120	74.63
130	210	70	110	150	73.70
130	210	70	110	200	72.78
130	210	70	120	120	73.09
130	210	70	120	150	72.47
130	210	70	120	200	71.86
130	210	70	130	120	72.08
130	210	70	130	150	71.67
130	210	70	130	200	71.25

Table 1: A partial, calculated Leff lookup table for 65 nm process technology and all numbers in the above table are in unit of nm.

The transistor drive currents of these test structures are measured and converted to the L_{eff}. Based on 65 nm test chip data, the lookup table is then generated and is as shown in Table 2.

Bent Field poly width (g)	Bent field poly length (e)	Poly width (a)	Bent field poly to diffusion spacing (f)	Diffusion width (w)	Effective poly width (Leff)
70	50	70	70	110	71.36
70	150	70	70	110	71.06
70	250	70	70	110	70.81
70	50	70	80	110	70.80
70	150	70	80	110	70.63
70	250	70	80	110	70.48
70	50	70	90	110	70.50
70	250	70	90	110	70.30
70	50	70	70	140	71.15
70	150	70	70	140	70.90
70	250	70	70	140	70.68
70	50	70	80	140	70.67
70	150	70	80	140	70.53
70	250	70	80	140	70.40
70	50	70	90	140	70.42
70	150	70	90	140	70.33
70	50	70	70	200	70.73
70	250	70	70	200	70.43
70	50	70	80	200	70.25

Table 2: A partial L_{eff} lookup table generated with 65 nm technology development test vehicle.

With the L_{eff} back-annotation-to-netlist flow chart is shown in Figure 4, the netlist is back-annotated with L_{eff} associated with parameters, a, e, f, and g. The back-annotated netlist is then used for post layout simulation. This approach takes the information in the L_{eff} lookup table (such as Table 1 or Table 2) as input. With the Nanoscope[6] software's pattern matching function, the transistor poly widths in the extracted netlist are modified if their layout environment match the parameters, a, e, f, g, and w in the L_{eff} lookup table. As opposed to some commercial applications[7, 8] that take physical simulation, full-chip based back-annotation, the transistor poly width, a, and transistor diffusion width (w) in this work can be selected and based on data from a simple L_{eff} lookup table so that only process sensitive transistors are back-annotation corrected and the data process time is therefore minimized. This approach also has the advantage for integrated circuit (IC) design houses that take the early engagement of an advanced process technology for their product developments even before they are mature for productions. Goals of the

transistor poly corner rounding target (i.e., L_{eff} in this work) can be set as that for a mature process so that both OPC and poly etching process can be optimized to achieve the goal during the process development. The product can in-parallel take the "targeted" L_{eff}'s in its design that reflects the mature process properties.
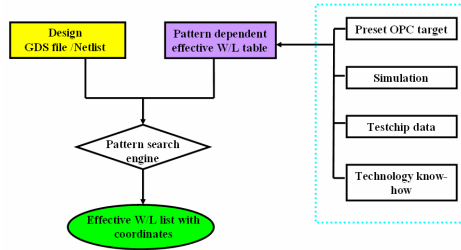

Figure 4: Process induced parameter back-annotation flow.

RESULT AND DISCUSSION

The Figures 5, 6, 7, and Table 2 appeared in this section are generated from the 65 nm process development test vehicle.

From the test chip data, it can be inferred that

- OPC provides more aggressive correction for wide bent field poly than that for narrow.
- OPC corrects less corner rounding for short bent field poly transistor than that for long.
- Transistor with wide diffusion width shows less poly rounding effect than that for narrow diffusion width transistors.

As shown in Figure 5, the corner rounding effect is reduced as the diffusion width becomes large. For the diffusion width, w, increased from 0.2 um to 0.26 um, the current degradation is reduced from -3.5% to -2.1%. The implies that the above mentioned bent field poly to diffusion rule can be flexibly adjusted to a small spacing for large diffusion width and to a large spacing for narrow diffusion width.
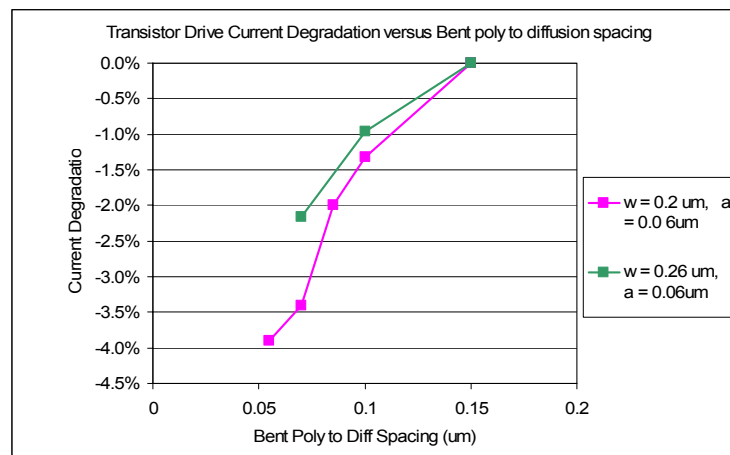
Figure 5: Transistor drive current versus bent field poly spacing for different diffusion widths. It can be clearly seen that wide transistor diffusion width reduces the poly corner rounding effect.

The Figure 6 shows the trend of more transistor drive current degradation for a short bent field poly transistor than that for long one. This indicates that OPC provides more corner corrections for long bent field poly transistor than that for a short one.
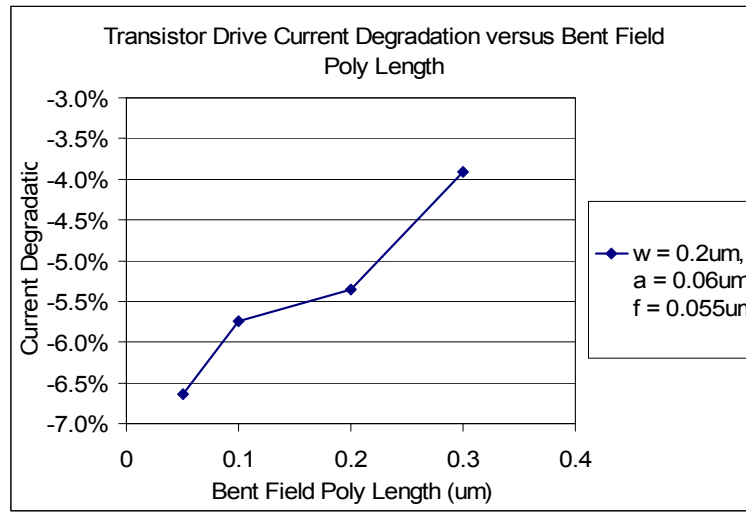

Figure 6: Transistor drive current degradation versus bent field poly length.

Bent field poly width also affects OPC approach in which OPC corrects poly corner more aggressively for wide bent field poly than that for narrow width bent field poly. The trend can be seen from the Figure 7 in which 65 nm process and OPC apply to the test chip in this experiment.
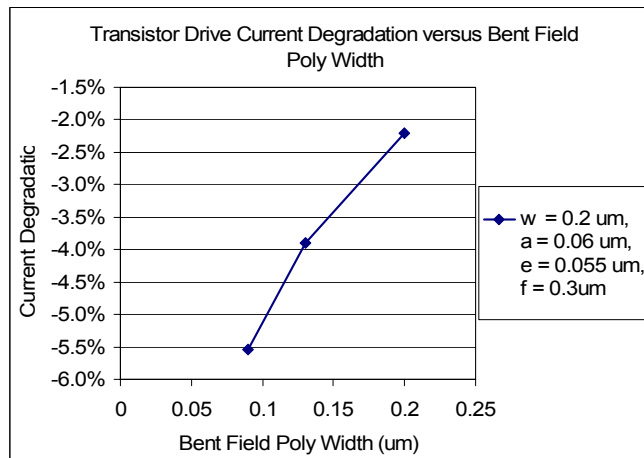

Figure 7: Transistor dive current degradation versus bent field poly width.

A ring oscillator (RO) is used as a test circuit. The information in the L_{eff} lookup tables back-annotates the RO netlist with Nanoscope software. Figures 8A and 8B show the netlist before and after the back-annotation. The L_{eff} effect to the RO delay is shown in Table 3. Due to the transistor drive current degradation, the example shows a 0.12% rise time and 0.34% fall time of RO delay changes respectively. Because the bent field poly to diffusion rule is relaxed in the ring oscillator layout, only a fraction of 1% change is observed.

```
O/MMNM58:B xnmosmlvt L=0.10u W=0.2750u ad=
15u ps=0.98u wrxd=0.555 wrxs=0.215
: 0/MMP5 XIint_interconnect_core/XIint_muxes_
 W=0.2u ad=0.042p as=0.027p ewp=0.716419 mx=1

:connect_core/XIint_muxes_48/XIint_byp_2_
 b vdd vdd xpmos L=0.14u W=0.12u ad=0.04575p
 wrxd=0.25 wrxs=0.25
: 0/MMNM47 XIint_interconnect_core/XIint_muxes_
 XIint_muxes_48/mcq_1<97> wr2mid<2> gnd
 )u PS=0.69u W=0.45u ewp=0.00733652 mx=1 wrxd=
```

Figure 8A: A sample portion of netlst of a ring oscillator before back annotation.

```
_0/MMNM58:B xnmosmlvt L=0.1005u W=0.2750u ad=
15u ps=0.98u wrxd=0.555 wrxs=0.215
x_0/MMP5 XIint_interconnect_core/XIint_muxes_
 W=0.2u ad=0.042p as=0.027p ewp=0.716419 mx=1

rconnect_core/XIint_muxes_48/XIint_byp_2_
 b vdd vdd xpmos L=0.1415u W=0.121u ad=0.04575p
 wrxd=0.25 wrxs=0.25
x_0/MMNM47 XIint_interconnect_core/XIint_muxes_
 XIint_muxes_48/mcq_1<97> wr2mid<2> gnd
 9u PS=0.69u W=0.45u ewp=0.00733652 mx=1 wrxd=
```

Figure 8B: A sample portion of netlst of a ring oscillator before back annotation. Highlighted device drawn poly width is modified based on the Leff lookup table.

	Before annotation	After annotation	% Change
Simulated Clock Rise time (ns)	24.28	24.31	-0.12%
Simulated Clock Rise time (ns)	26.46	26.55	-0.34%

Table 3: Circuit performance before and after back-annotation of the transistor poly width.

SUMMARY AND FUTURE PERSPECTIVE

A procedure in IC design for correcting process induced layout dimension change is presented. The procedure corrects process induced systematic layout variations and is proven working with a ring oscillator circuit. From the ring oscillator circuit test, a ~ 0.12 % larger than designed poly width is modified to the transistors. This therefore reflects the actual, uncorrectable process induced layout dimension changes.

Aside from the poly corner rounding, process induced variations, such as L-shape transistor diffusion rounding and layout style induced stress changes, can also back-annotate the design parameters in the netlist that reflects the design layouts with wafer process properties.

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